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PATENT ABSTRACTS OF JAPAN

(11)Publication number : 07-111318
(43)Date of publication of application : 25.04.1995

(51)Int.Cl. H01L 27/10
G11C 11/22
H01L 27/04
H01L 21/822
H01L 21/8242
H01L 27/108

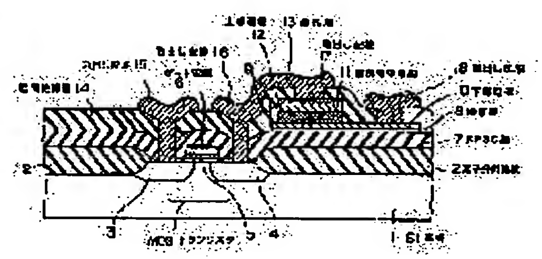
(21)Application number : 05-254378
(22)Date of filing : 12.10.1993

(71)Applicant : OLYMPUS OPTICAL CO LTD
SYMMETRICS CORP

(72)Inventor : WATANABE HITOSHI
KURODA YOSHIKI
TADOKORO KAORU

(54) FERROELECTRIC MEMORY

(57)Abstract:
PURPOSE: To stop the reducing reaction and the degeneration of the surface of an oxide ferroelectric body, and to prevent the peeling between the ferroelectric thin film and the upper and the lower electrodes in a MOS sintering process.
CONSTITUTION: This ferroelectric memory is provided with a semiconductor substrate 1, a dielectric thin film capacitor 9 formed by successively laminating a lower electrode 10, an oxide ferroelectric thin film 11 and an upper electrode 12 on the substrate 1, and a protective film 12 which is mainly composed of a nitride thin film of an aluminum, silicon or titanium coating the surface of the capacitor 9.



LEGAL STATUS

[Date of request for examination] 06.10.2000
[Date of sending the examiner's decision of rejection] 07.05.2002
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]
[Date of final disposal for application]
[Patent number]
[Date of registration]
[Number of appeal against examiner's decision of rejection]
[Date of requesting appeal against examiner's decision of rejection]
[Date of extinction of right]

JP,07-111318,A

CLAIMS

[Claim(s)]

[Claim 1] Ferroelectric random-access memory characterized by providing a protective coat which uses as main components aluminum and silicon which were prepared on a semiconductor substrate and this substrate and were covered by a ferroelectric thin film capacitor constituted by a lower electrode, an oxide ferroelectric thin film, and an up electrode carrying out a sequential laminating, and this capacitor front face, or a nitride thin film of titanium.

[Claim 2] Ferroelectric random-access memory given in a claim to which said protective coat is characterized by oxide ferroelectric which constitutes a ferroelectric thin film capacitor, this presentation, or being what uses as main components an oxide thin film which shares a configuration element a part.

[Claim 3] Ferroelectric random-access memory according to claim 1 to which said protective coat is characterized by being a partial crystal film or an amorphous film.

[Claim 4] Ferroelectric random-access memory according to claim 1 characterized by preparing a protective coat and an undercoating layer of this presentation and this structure between said semiconductor substrate and a ferroelectric thin film capacitor.

[Claim 5] Ferroelectric random-access memory according to claim 1 characterized by for the transistor elements separately prepared on said ferroelectric thin film capacitor and semiconductor substrate separating an interlayer insulation film by which the laminating was carried out to said protective coat and/or this protective coat, and connecting them to them electrically with a laminating wiring electrode of alumimium nitride and an aluminum-silicon alloy.

[Claim 6] Ferroelectric random-access memory according to claim 1 characterized by for said oxide strong ferroelectric thin film consisting of a bismuth stratified perovskite mold compound which has a presentation expressed by the following general formula (1), and having a concentration gradient of the following element B in the direction of thickness, and an element B containing richly in an interface with an up electrode.

(Bi 2O2) 2+(Am-1 Bm O3m+1)2- -- (1)

However, be based on one or an arbitration ratio which consists of base chosen from from among A=Bi, and Pb, Ba, Sr, calcium, Na, K and Cd, and combine with it. Be based on one or an arbitration ratio which consists of base chosen from from among B=Ti, and Nb, Ta, W, Mo, Fe, Co and Cr, and combine with it. The natural number of m=1-5.

[Claim 7] Ferroelectric random-access memory according to claim 1 characterized by for said bismuth stratified perovskite mold compound being SrBi2 2 (Tax Nb 1-x) O9 (x=0-1.0), and an element B being Ta or Nb.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] Especially this invention relates to the ferroelectric random-access memory using the remanence property of an oxide ferroelectric thin film about ferroelectric random-access memory.

[0002]

[Description of the Prior Art] Conventionally, the ferroelectric compound is applied to many fields using the unique electrical property. For example, it is applied in many fields [the light modulation element which used an infrared sensor, a PAIRO vidicon, or the electro-optical effect for the piezo-electric filter using piezoelectric, or the ultrasonic transducer again using pyroelectricity, an optical shutter, etc.]. The electron device which furthermore used the thin film of these materials is also devised, and examination of thin-film-izing is made energetically. Especially the non-volatile memory device of ferroelectric thin film capacitor loading using the stability of a remanence is a field which attracts attention most against the background of the densification of the latest storage capacity, and high integration

competition.

[0003] As a representation material currently competed for which and studied according to such versatility, a series of lead content multiple oxide ferroelectrics, such as PZT (titanic-acid lead zirconate) and PLZT (titanic-acid zirconic acid lanthanum lead), are mentioned, and examination of utilization is continued by many researchers over many years.

[0004] moreover, the outstanding fatigue-proof property which also exceed the several more or more figures thin film of a bismuth stratified perovskite mold oxide ferroelectric by the informational count of record elimination as other promising dielectric materials as compared with thin films which be the conventional main materials, such as PZT and PLZT, can be show, and it can apply to the non-volatile memory device which have high endurance ability, other electrons, and an optical device.

[0005] The above-mentioned ferroelectric thin film can be formed by the physical forming-membranes methods, such as reaction vacuum deposition of the spatter metallurgy group using the ceramic target calcinated beforehand, the CVD method which carries out the gaseous-phase deposition of the organic metal compound, the sol gel process which forms membranes by applying the same compound solution, the MOD method, etc.

[0006] Generally, a ferroelectric material has the hysteresis characteristic of a remanence and can memorize data as nonvolatile memory using this property. The ferroelectric random-access memory 1 using such a ferroelectric material The switching element which consists of MOS transistors etc. as shown in drawing 1 , On the substrate 3 which consists of a silicon semiconductor, for example in which the circumference elements 2, such as amplification amplifier, were formed The ferroelectric thin film capacitor 7 which comes to carry out the laminating of the lower electrode 4 using platinum etc., the ferroelectric thin film 5, and the up electrode 6 one by one is formed, and the interlayer insulation film 8 which consists of silicon oxide with a spatter or a CVD method further is formed, and between elements is further connected with the wiring electrode 9, and it is constituted.

[0007] The protective coat (not shown) for protecting the under-coating layer 10 and ferroelectric thin film capacitor for raising the substrate adhesion of the lower electrode 4 from various environmental variations in addition to the above basic structure etc. is prepared if needed. Here, as a protective coat of the conventional ferroelectric random-access memory, the following are proposed, for example.

(1) It is Ti3 N4 to a ferroelectric PZT thin film and up inter-electrode one. It is direct Si3 N4 about PZT at the same time it prepares a layer. By covering with a layer, the oxygen desorption from PZT is prevented and a switching fatigue property is improved (JP,2-183569,A).

(2) By carrying out the laminating of a 1st electric conduction film [which consists of platinum or rose JIUMU], titanium, titanium nitride, and titanium-tungsten alloy, and the 2nd electric conduction film which consists of molybdenum silicide, and considering as a capacitor up electrode, prevent alloying of an aluminum wiring electrode and the 1st conductive layer, and heat treatment in an after process is enabled (JP,2-90606,A).

[0008]

[Problem(s) to be Solved by the Invention] however, the ferroelectric random-access memory mentioned above -- the manufacture process -- setting -- a spatter and SUPION -- it passes through the comparatively hot heat treatment process which amounts to 600-900 degrees C indispensable to crystallization of the ferroelectric thin film formed by law, or many lattice defects are produced in the single crystal structure of a semiconductor silicon substrate by the plasma contamination by the processing processes by the high energy beam and reactant plasma etching, such as ion milling, and this degrades the MOS transistor property on a substrate.

[0009] For this reason, it is H2 by performing 350-450-degree C heat treatment (MOS sinter) into a hydrogen mixing nitrogen gas (foaming gas) ambient atmosphere in a final process for a property improvement. It is necessary to restore the MOS property which carried out termination of the defect of the dangling bond generated in single crystal silicon using reducibility, and deteriorated.

[0010] However, the platinum which is ******** is used to hydrogen as an electrode material for ferroelectric thin films. According to therefore, a reduction operation of the hydrogen which carried out diffusion passage of the above-mentioned interlayer insulation film and the up electrode, and reached to the interface and the capacitor

side of an up electrode and a ferroelectric thin film in the heat treatment process in a reducing atmosphere The oxide near the interface causes an oxidation reduction reaction, or decomposes, and originate in the chemical change in this interface, and adhesion with an up electrode falls or an up electrode is pushed up with oxygen, water, etc. which are a resultant. There was a problem which generates exfoliation in the interface of an up electrode and a ferroelectric thin film as a result.

[0011] Moreover, it was thought that osmosis in the interior of a device of a reducing atmosphere occasionally attained to a lower electrode through the capacitor side, and when the aluminum-Si wiring electrode with which comparatively big internal stress tends to remain was used, nonconformity the whole capacitor exfoliates from the semiconductor substrate itself might also be produced. A new cure has been needed when such a problem constitutes ferroelectric random-access memory combining a ferroelectric thin film capacitor and a silicon semiconductor device.

[0012] This invention was made in consideration of such a situation, and aims at offering the structure where a ferroelectric thin film and vertical inter-electrode exfoliation can be prevented in the MOS sinter process under a reducing atmosphere in the ferroelectric random-access memory which consists of an oxide ferroelectric thin film capacitor and a silicon device.

[0013]

[Means for Solving the Problem] This invention is ferroelectric random-access memory characterized by providing a protective coat which uses as main components aluminum and silicon which were prepared on a semiconductor substrate and this substrate and were covered by a ferroelectric thin film capacitor constituted by a lower electrode, an oxide ferroelectric thin film, and an up electrode carrying out a sequential laminating, and this capacitor front face, or a nitride thin film of titanium.

[0014] In this invention, aluminum which is the material of said protective coat, silicon, or a nitride thin film of titanium has comparatively high film density, hydrogen gas is not made to penetrate stably and easily also chemically as compared with an oxide, but, as for thickness, it is desirable to make it the range of 20nm - 100nm.

[0015] Said nitride thin film can be easily formed by the various well-known forming-membranes methods, for example, dc, or well-known rf spatter, ion beam deposition, CVD method, and occasionally using a sol gel process.

[0016] in this invention, main components have pointed out an effect of preventing diffuse transmission of reducibility gas, and what is been the reinforcement layer prepared in order to improve adhesion with said nitride thin film and up electrode, or an interlayer insulation film as other components is said. Usually, as a reinforcement layer in a case of carrying out the laminating of a nitride thin film and other thin films, an oxide thin film of a share metal is suitable. Especially, the electrode exfoliation prevention effect of a nitride thin film is not spoiled by existence of an oxide reinforcement layer.

[0017] In addition, among the above-mentioned nitrides, since a nitride of titanium and aluminum can maintain conductivity, it can cover the whole surface of a capacitor up electrode, and can raise a hydrogen shielding effect. Since it is insulation, it is necessary to dig a contact hole for joining a wiring electrode and an up electrode electrically in the case of silicon nitride, and to make it penetrate. Therefore, since a protective coat is removed, although an effect as a protective coat falls, since only a surface integral of a contact hole can carry out the direct coat of the capacitor side, a surroundings lump by the side can be prevented. Moreover, a capacitor is not protected by one kind of protective coat, but an up electrode side may be carried out with a nitride of aluminum or titanium, and the concomitant use coat of the side may be carried out with a silicon nitride.

[0018] In this invention, it is also an effective means to cover an up electrode surface with a ferroelectric material which constitutes a ferroelectric thin film capacitor which is protected, and which is an object as protective coats other than the above-mentioned metal nitride thin film, this presentation, or an oxide ferroelectric thin film which shares a configuration element in part. Hydrogen which reached to a protective coat front face which consists of this oxide ferroelectric that carried out diffuse transmission of a wiring electrode and the interlayer insulation film, and was prepared on an up electrode is consumed by reduction reaction of an oxide ferroelectric, and does not reach to the interior over an up electrode.

[0019] Therefore, most desirable one as a protective coat material in this case is equivalent

also on the crystal structure also in presentation, and reactivity with hydrogen is also a thin film equal to a capacitor ferroelectric thin film. However, when several sorts of electrodes and a metal layer exist on both sides of this on structure of a memory device, trouble may be caused to the actuation of a device itself as a protective coat is not a mere dielectric but a ferroelectric. In such a case, it is desirable by making burning temperature at the time of protective coat membrane formation below into crystallization temperature of a ferroelectric an amorphous substance or to control a manifestation of a stop and a ferroelectricity for carrying out partial crystallization.

[0020] thus, the presentation as an oxide ferroelectric which not necessarily constitutes a ferroelectric thin film capacitor with same thin film material in which an effect which inhibits internal diffusion beyond it by reacting with a reducibility gas oneself is shown -- not but -- ** -- good -- for example, a part -- a compound and a specific element which replaced an element were removed -- the same object can be presented also with a compound. For example, SrBi2 Ta 2O9 With a device which uses a thin film as a capacitor material, it is SrTa 2O6. SrBi2 Nb 2O9 Effect also with a thin film sufficient as a protective coat is given. Also at this time, it is natural that they may be crystallization films, may be partial crystallization films, or may be amorphous films further as long as these protective coats have oxidized enough.

[0021] Furthermore, the above-mentioned protective coat can give very same effect for a configuration which covers the whole substrate from on an interlayer insulation film which covers not only an outside surface of a ferroelectric capacitor up electrode but a capacitor group directly (as an under-coating layer of a wiring electrode). In addition, this protective coat and an under-coating layer of this presentation and this structure may be prepared in a silicon substrate surface, a capacitor lower electrode may be formed on it, and ferroelectric random-access memory may be constituted according to above-mentioned structure. This under-coating layer covers a reducibility gas around which it turns from the capacitor side, and shows an effect of preventing exfoliation from a lower electrode.

[0022] Moreover, effect of a reduction gas to a ferroelectric thin film capacitor can be prevented also by covering the whole surface surface of ferroelectric random-access memory which even a wiring electrode constituted as a natural configuration using a protective coat of this invention. in this case, a protective coat -- a multilayer -- you may be -- for example, a silicon oxide film -- minding -- also preparing -- a layer of still more nearly same silicon oxide may be prepared on the surface of a protective coat as a configuration of reverse. since the hydrogen permeation prevention effect by protective coat was too large to supply sufficient amount of hydrogen for property recovery to the MOS transistor section in this configuration, a protective coat on the MOS transistor section was removed -- it can also constitute.

[0023] Although structure of ferroelectric random-access memory containing a protective coat of above-mentioned electrode exfoliation prevention does not choose a class of ferroelectric material, when an oxide ferroelectric thin film consists of a bismuth stratified perovskite mold compound which has a presentation expressed by the following general formula (1), the remarkable exfoliation prevention effect can be acquired also by adjusting the presentation of a ferroelectric material itself. whether B site element in a formula (1) is in a metal condition or is in an oxide condition -- the any -- although -- it is the element used abundantly as a junctional zone between layers from which it excels in adhesion with silicon oxide or other metals, and an electrode metal, an under-coating layer, an thermal expansion coefficient, and a lattice constant differ.

[0024] Here, membranes can be beforehand formed in B overelement at the time of membrane formation of a ferroelectric thin film, and the many can form an oxide particle of the element B which segregated in a thin film front face simultaneously by calcinating at an elevated temperature by the same ferroelectric phase and superfluous combination as a film of stoichiometric composition. Even if it forms a stoichiometric ratio presentation in a lower layer, it forms a multilayer of an element B superfluous presentation in the upper layer and surface segregation of the same element B calcinates this, it is realizable.

[0025]

(Bi 2O2) 2+(Am-1 Bm O3m+1)2- -- (1)

However, be based on one or an arbitration ratio which consists of base chosen from from among A=Bi, and Pb, Ba, Sr, calcium, Na, K and Cd, and

combine with it. Be based on one or an arbitration ratio which consists of base chosen from from among B=Ti, and Nb, Ta, W, Mo, Fe, Co and Cr, and combine with it.

[0026] The natural number of m=1-5. in this way, in a thin film capacitor which consisted of ferroelectric thin films which consist of a bismuth stratified perovskite mold compound which has a concentration gradient of Element B in the acquired direction of thickness, and Element B contains richly in an interface with an up-electrode Although a part of crystal structures are returned, it is destroyed and some amount lowering of remanences and an increment in a coercive electric field are seen in foaming processing in a reducing atmosphere B element oxide which is a segregation component, or when [its] a reductant reinforces cementation to an electrode metal also including an alloying reaction in part, an effect of preventing exfoliation of an electrode is generated. Especially when a capacitor ferroelectric is the bismuth stratified perovskite mold compound expressed with SrBi2 2 (Tax Nb 1-x) O9 (x=0-1.0) and Element B is Ta or Nb, ferroelectric random-access memory electrode bonding strength excelled [ferroelectric random-access memory] in an absolute value list of the amount of remanences can be constituted.

[0027]

[Function] According to this invention, the reduction reaction of an oxide ferroelectric front face and deterioration can be prevented preparing the protective coat which prevents internal diffusion osmosis of reducibility gas in a front face, the capacitor side, etc. of an up electrode of a ferroelectric thin film capacitor, or by [of a ferroelectric material thin film] blending a configuration element superfluously in part. Moreover, it can prevent that an up electrode and a lower electrode exfoliate from a ferroelectric thin film by foaming processing like before.

[0028]

[Example] Hereafter, the example of this invention is explained with reference to a drawing with the example of a comparison.

(Example 1) Drawing 1 is referred to. One in drawing is the silicon substrate by which the element isolation region 2 was formed in the front face. The source field 3 and the drain field 4 are formed in the element field of the substrate 1 surrounded in said element isolation region 2, and the gate electrode 6 is further formed through the gate insulator layer 5 on these fields 3 and the substrate 1 between four. Here, said source drain fields 3 and 4 and the gate electrode 6 are generically called an MOS transistor.

[0029] All over substrate 1 including said element isolation region 2, the BPSG (boron phosphorus dope silicon oxide) film 7 is formed. On the BPSG film 7 on said element isolation region 2, the ferroelectric thin film capacitor 9 is formed through the undercoating layer (glue line) 8 of 20nm of thickness, such as titanium. This ferroelectric thin film capacitor 9 is formed from the up electrode 12 of 200nm of thickness which consists of a ferroelectric thin film 11 by which sequential formation was carried out, and Pt on the lower electrode 10 of 200nm of thickness which consists of Pt, and this lower electrode 10, and consists of protective coats 13 of 50nm of thickness on the up electrode 12. Said ferroelectric thin film 11 consists of a sol gel thin film of PZT (40/60).

[0030] The interlayer insulation film 14 is formed on said BPSG film 7 containing said ferroelectric thin film capacitor 9. Opening is formed in said interlayer insulation film 14 and the BPSG film 7 corresponding to the source field 3 and a drain field of said MOS transistor, and the source drawing wiring 15 and the drain drawing wiring 16 are formed in this opening. Moreover, opening is formed also in the up protective coat 13 of said ferroelectric thin film capacitor 9, and said interlayer insulation film 14 corresponding to the lower electrode 10, and the drawing wiring 17 for up electrodes and the drawing wiring 18 for lower electrodes are formed in these openings. Said drain drawing wiring 16 and the drawing wiring 17 for up electrodes are connected electrically. Moreover, each above-mentioned drawing wiring consists of aluminum-Si.

[0031] The ferroelectric random-access memory of the configuration of drawing 1 is manufactured as follows.

(1) First, with well-known technology, such as semiconductor ultra-fine processing technology, after forming the element isolation region 2 in the front face of a substrate 1, the MOS transistor which consists of the source field 3, a drain field 4, a gate electrode 6, etc. was formed in the element field surrounded in this element isolation region 2. It continued and the lower electrode 10 of 200nm of thickness was formed through the glue line 8 of 20nm of thickness after ** in which the BPSG film 7 was formed all over the substrate, by dc spatter on said element isolation region 2. Next,

adjustment, spin coat spreading of the sol gel PZT precursor solution which performed partial hydrolysis, desiccation, and temporary quenching were repeated to predetermined concentration and a presentation, the temporary-quenching thin film of request thickness was formed, baking processing was performed at the last in a temperature predetermined in the inside of an oxygen ambient atmosphere, and the ferroelectricity PZT thin film (ferroelectric thin film) 11 of 300nm of thickness was obtained. It pulled and continued and the spatter of the up electrode material of the lower electrode 10 and this thickness (200nm) was carried out on said ferroelectric thin film 11, after forming the protective coat 13 which consists of alumimium nitride (AlN) of 50nm of thickness by dc spatter on the up electrode 10 further, processing of each electrode and the ferroelectric thin film 11 was performed in ion milling, and the ferroelectric thin film capacitor 9 was formed.

[0032] (2) Next, the spin coat of the spin-on glass was carried out to the whole surface, it calcinated by having dried according to the predetermined process, and the interlayer insulation film 14 of 400nm of thickness was formed. It continued and the contact hole was formed in said interlayer insulation film 14 corresponding to the source field 3 of said MOS transistor, and the drain field 4, the BPSG film 7 and the protective coat 13 of the ferroelectric thin film capacitor 9, and the interlayer insulation film 14 corresponding to the lower electrode 10, respectively. Furthermore, the wiring material film of 300nm of thickness which becomes the whole surface from aluminum-Si by the spatter was formed, patterning of this wiring material film was carried out using the well-known sentiment dirty method, the source drawing wiring 15, the drain drawing wiring 16, the drawing wiring 17 for up electrodes, and the drawing wiring 18 for lower electrodes formed in said each contact hole, and the ferroelectric random-access memory by which the MOS transistor was electrically connected with the ferroelectric thin film capacitor was manufactured.

[0033] Thus, the ferroelectric random-access memory of an example 1 consists of MOS transistor 6 and the ferroelectric thin film capacitor 9 which were connected electrically. Said MOS transistor 6 consists of the source fields 3, the drain fields 4, the gate electrodes 6, etc. which were formed in the element field. Said ferroelectric thin film capacitor 9 consists of the lower electrodes 10, the ferroelectricity PZT thin films (ferroelectric thin film) 11, and the up electrodes 12 which were formed through the glue line 8 on the BPSG film 7 on the element isolation region 2. However, since [which was covered with the protective coat 13 which consists of AlN] it is constituted, the upper surface of said capacitor 9, especially the upper surface of the up electrode 12 can intercept internal transparency of reducibility gas, and can prevent the electrode exfoliation resulting from the reduction reaction of ferroelectric thin film 11 front face, and this.

[0034] (Example 2) This example 2 is the completely same configuration except for the point using the protective coat which consists of titanium nitride (Ti_3N_4) of 50nm of thickness compared with an example 1. According to the ferroelectric random-access memory concerning the example 2 using the protective coat which consists of titanium nitride, the same effect as an example 1 is acquired.

[0035] (Example 3) <u>Drawing 2</u> is referred to. However, <u>drawing 1</u> and said division material attach a same sign, and explanation is omitted. 21 in drawing is a protective coat of 50nm of thickness which becomes not only the upper surface of the ferroelectric thin film capacitor 9 but the side from the silicon nitride (Si_3N_4) by which coat formation was carried out. After this protective coat 21 forms the ferroelectric thin film capacitor 9, it is formed in the whole surface by forming silicon nitride by dc spatter.

[0036] Since the protective coat 21 which consists of silicon nitride is formed not only in the upper surface of the ferroelectric thin film capacitor 9 but in the side according to the above-mentioned example 3, the surroundings lump by the capacitor side of reducibility gas can be prevented.

[0037] (Example 4) <u>Drawing 3</u> is referred to. However, <u>drawing 1</u> , and 3 and said division material attach a same sign, and explanation is omitted. It is the feature that this example 4 is the configuration which combined the protective coat 13 which consists of AlN formed only in the upper surface of the ferroelectric thin film capacitor 9, and the protective coat 21 which consists of silicon nitride which covers said a part of protective coat 13 and the side of the ferroelectric thin film capacitor 9. According to the above-mentioned example 4, the upper surface of the up electrode 12 of the ferroelectric thin film capacitor 9 can be covered with the combination of two kinds of protective coats 13 and 21, and a

hydrogen shielding effect can be raised, and also the surroundings lump by the capacitor side of reducibility gas can be prevented.

[0038] (Example 5) This example 5 of other configurations is completely the same except for the point made into the two-layer structure of the protective coat which consists of silicon oxide (SiO_2) of 50nm of thickness, and the protective coat which consists of silicon nitride (Si_3N_4) of 50nm of thickness on this protective coat compared with an example 3.

[0039] (Example 6) Drawing 4 is referred to. However, drawing 1 and said division material attach a same sign, and explanation is omitted. It differs in that the protective coat 41 which consists of AlN was formed also on the interlayer insulation film 14 around a contact hole besides the protective coat 13 which this example 6 becomes from AlN illustrated by drawing 1 compared with an example 1. Since it not only covers a protective coat 13 on the upper surface of the up electrode 12 of the ferroelectric thin film capacitor 9, but the whole substrate is covered from on the interlayer insulation film 14 which covers a capacitor group directly according to the above-mentioned example 6, the hydrogen shielding effect to an up electrode can be raised, and also the surroundings lump by the capacitor side of reducibility gas can be prevented.

[0040] (Example 7) Drawing 5 is referred to. However, drawing 1 and said division material attach a same sign, and omit explanation. This example 7 has completely same composition except for the point of having formed the protective coat 51 of 50nm of thickness which consists of AlN between the BPSG film 7 and a glue line 8, compared with the example 1. Here, said protective coat 51, a glue line 8, and the lower electrode 10 may be simultaneously formed by patterning with one mask, and may be formed at another process.

[0041] (Example 8) It compares with an example 3 and this example 8 is bismuth stratified perovskite mold compound SrBi2 Ta 2O9 as a ferroelectric thin film of a ferroelectric thin film capacitor. It is ferroelectricity SrBi2 Ta 2O9 of 80nm of thickness as the point using an MOD thin film (250nm of thickness), and a protective coat. The points using a thin film differ. Here, said protective coat is SrBi2 Ta 2O9. One-layer spin coat spreading of the MOD precursor solution was carried out, desiccation and temporary quenching were performed, the temporary-quenching thin film was formed, and it obtained by subsequently performing baking processing in 800 degrees C in an oxygen ambient atmosphere.

[0042] (Example 9) It compares with an example 3 and this example 9 is bismuth stratified perovskite mold compound SrBi2 Ta 2O9 as a ferroelectric thin film of a ferroelectric thin film capacitor. The point using an MOD thin film (250nm of thickness) differs from the point using the amorphous film of the non-ferroelectricity oxide of 80nm of thickness as a protective coat. Here, said protective coat is SrBi2 Ta 2O9. One-layer spin coat spreading of the MOD precursor solution was carried out, desiccation and 400-degree-C temporary quenching were performed, and the temporary-quenching thin film was formed and pulled, and in 600 degrees C sufficiently lower than the crystallization temperature of the above-mentioned compound, baking processing was performed in the continuation oxygen ambient atmosphere, and it obtained by burning enough and fastening.

[0043] (Example 10) It compares with an example 3 and this example 10 is bismuth stratified perovskite mold compound SrBi2 Ta 2O9 as a ferroelectric thin film of a ferroelectric thin film capacitor. The point using an MOD thin film (250nm of thickness) differs from the point using the crystalline thin film of 80nm of thickness as a protective coat. Here, said crystalline thin film was obtained by carrying out one-layer spin coat spreading of the MOD precursor solution of ferroelectric SrBi2 Ta 2O9 of a thin film capacitor, and SrTa 2O6 (tantalic acid strontium) which consists of common elements in part, performing desiccation and 400-degree-C temporary quenching, forming and pulling a temporary-quenching thin film and performing baking processing in 800 degrees C in a continuation oxygen ambient atmosphere.

[0044] (Example 11) It compares with an example 3 and this example 11 is bismuth stratified perovskite mold compound SrBi2 Ta 2O9 as a ferroelectric thin film of a ferroelectric thin film capacitor. It is SrBi2 Nb 2O9 of the ferroelectric nature of 80nm of thickness as the point using an MOD thin film (250nm of thickness), and a protective coat. The points using a thin film differ. Here, said ferroelectric nature thin film is SrBi2 Nb 2O9. It obtained by carrying out one-layer spin coat spreading of the MOD precursor solution which has a presentation, performing

desiccation and ******, forming and pulling a temporary-quenching thin film and performing baking processing in 850 degrees C in a continuation oxygen ambient atmosphere.

[0045] (Example 12) Drawing 6 is referred to. However, drawing 1 and drawing 5 , and said division material attach a same sign, and omit explanation. It compares with an example 1 and this example 12 is ferroelectric nature SrBi2 Ta 2O9 of 80nm of thickness as a protective coat to the front face of the BPSG film 7. While using a thin film 61, it is ferroelectric nature SrBi2 Ta 2O9 of 100nm of thickness on the up electrode 12 of a capacitor. Except for the point of having formed the thin film 62, it has completely same composition. Here, said thin film 61 is SrBi2 Ta 2O9. It obtained by carrying out one-layer spin coat spreading of the precursor solution, performing desiccation and ******, forming and pulling a temporary-quenching thin film and performing baking processing in 800 degrees C in a continuation oxygen ambient atmosphere. Moreover, it is SrBi2 Ta 2O9 like [said thin film 62] a thin film 61. It obtained by carrying out one-layer spin coat spreading of the precursor solution, performing desiccation and temporary quenching, forming and pulling a temporary-quenching thin film and performing baking processing in 800 degrees C in a continuation oxygen ambient atmosphere.

[0046] (Example 13) This example 13 is overtantalum ferroelectricity SrBi2 Ta 2O9 compared with an example 1 as the point of not preparing a protective coat in an up electrode, and a ferroelectric thin film. Except for the point using a thin film, structure is the same. Here, said thin film is obtained as follows. Namely, SrBi2 Ta 2O9 after forming a lower electrode It obtained by adjusting a spreading solution, carrying out spin coat spreading so that a tantalum may become superfluous [20 mol %] to a stoichiometric ratio about a precursor solution, repeating desiccation and temporary quenching, forming and pulling a temporary-quenching thin film, and performing baking processing in 800 degrees C in a continuation oxygen ambient atmosphere. Thus, when the crystal structure was analyzed for said obtained thin film by the X diffraction, ICP analysis, electron microscope observation, etc. and the thin film component analysis was performed, inside the thin film, the paraelectric phase which is mainly concerned with tantalum oxide to a ferroelectric phase was intermingled, and it was checked in the thin film front face that tantalum oxide is segregating mostly.

[0047] (Example 14) As for this example 14, an example 13 differs only from a ferroelectric thin film. Here, this ferroelectric thin film is obtained as follows. Namely, SrBi2 Ta 2O9 after forming a lower electrode Spin coat spreading of the stoichiometric ratio solution of a precursor is carried out. Repeat the cycle of desiccation and temporary quenching twice, form a temporary-quenching thin film, and the 2nd precursor solution adjusted so that a tantalum might become superfluous [20 mol %] to a stoichiometric ratio at the last layer is applied. It obtained desiccation and by carrying out temporary quenching, forming and pulling a temporary-quenching thin film, and performing baking processing in 800 degrees C in a continuation oxygen ambient atmosphere. thus, the place which analyzed the crystal structure for said obtained thin film by the X diffraction, ICP analysis, electron microscope observation, etc., and performed the thin film component analysis -- most thin films -- SrBi2 Ta 2O9 of a ferroelectric phase it is -- the segregation of tantalum oxide was checked only on the thin film front face.

(Example 1 of a comparison) Drawing 7 is referred to. However, drawing 1 and said division material attach a same sign, and omit explanation. The example 1 of a comparison has the completely same composition except for the point of having not prepared the protective coat, compared with drawing 1 . However, it is Pb(Zr0.4 Ti0.6) O3 of 300nm of thickness as a ferroelectric. The thin film was used.

[0048] (Example 2 of a comparison) The example 2 of a comparison has the completely same composition except for the point of having not prepared the protective coat, compared with drawing 1 . However, it is SrBi2 Ta 2O9 of 300nm of thickness as a ferroelectric. The thin film was used.

[0049] (Example 15) 2OSrBi2 Ta9 thin film in which the thin film capacitor ferroelectric was formed on the example 2 (SrBi2 Ta2 O9 finishing [the ferroelectric random-access memory using a thin film, and wiring electrode pattern formation]) of a comparison -- forming membranes -- subsequently -- the inside of an oxygen ambient atmosphere -- 600 degrees C -- setting -- baking processing -- carrying out -- the amorphous nature of 100nm of thickness, and SrBiof non-dielectric2 Ta 2O9 Surface coating was

carried out with the thin film. Then, only the portion corresponding to the MOS transistor section carried out the opening of the MOS contact hole to which the wiring electrode was exposed to this protective coat, and the ferroelectric random-access memory of drawing 8 was obtained. In addition, in drawing 8 , 81 shows a contact hole and 83 shows a protective coat.

[0050] 425 degrees C and MOS sinter processing for 30 minutes were performed in the nitrogen gas (FO MIG gas) ambient atmosphere which contains 5% of hydrogen for the ferroelectric random-access memory concerning the above-mentioned example and the examples 1 and 2 of a comparison all over a diffusion furnace. Consequently, in the examples 1 and 2 of a comparison, almost all capacitors caused exfoliation in the ferroelectric thin film-up electrode interface. On the other hand, in all the examples, electrode exfoliation was not observed, but the strong dielectric-hysteresis property and MOS transistor property was also good, and ferroelectric random-access memory operated thoroughly.

[0051] in addition, in each above-mentioned example, although an example of materials, such as a lower electrode, a ferroelectric thin film, an up electrode, a protective coat, and drawing wiring, was described, it comes out not to mention not being limited to these materials.

[0052]

[Effect of the Invention] As explained in full detail above, the reduction reaction of an oxide ferroelectric front face and deterioration are prevented preparing the protective coat which prevents internal diffusion osmosis of reducibility gas according to this invention, or by [of a ferroelectric material film], blending a configuration element superfluously in part, and a ferroelectric thin film and vertical inter-electrode exfoliation are prevented in an MOS sinter process like before, and the ferroelectric random-access memory with which practical use can be presented can be offered.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] The cross section of the ferroelectric random-access memory concerning the example 1 of this invention.

[Drawing 2] The cross section of the ferroelectric random-access memory concerning the example 3 of this invention.

[Drawing 3] The cross section of the ferroelectric random-access memory concerning the example 4 of this invention.

[Drawing 4] The cross section of the ferroelectric random-access memory concerning the example 6 of this invention.

[Drawing 5] The cross section of the ferroelectric random-access memory concerning the example 7 of this invention.

[Drawing 6] The cross section of the ferroelectric random-access memory concerning the example 12 of this invention.

[Drawing 7] The cross section of the ferroelectric random-access memory concerning the example 1 of a comparison.

[Drawing 8] The cross section of the ferroelectric random-access memory concerning the example 15 of this invention.

[Description of Notations]

1 -- Silicon substrate, 2 -- Element isolation region, 3 [5 -- Gate insulator layer, 6 / 8 / -- Lower electrode, / 11 / 13, 21, 41, 51, 61, 82 -- A protective coat,, 15-18 -- Drawing wiring, / -- A ferroelectric thin film, 12 -- Up electrode, / -- A glue line 9 -- A ferroelectric thin film capacitor 10 / -- A gate electrode, 7 -- BPSG film,] -- A source field, 4 -- Drain field

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CORRECTION OR AMENDMENT

[Official Gazette Type] Printing of amendment by the convention of 2 of Article 17 of patent law
[Category partition] The 2nd partition of the 7th category
[Date of issue] August 31, Heisei 13 (2001. 8.31)

[Publication No.] JP,7-111318,A
[Date of Publication] April 25, Heisei 7 (1995. 4.25)
[Year copy format] Open patent official report 7-1114
[Filing Number] Japanese Patent Application No. 5-254378
[The 7th edition of International Patent Classification]
H01L 27/10 451
G11C 11/22
H01L 27/04
21/822
21/8242
27/108
[FI]
H01L 27/10 451
G11C 11/22
H01L 27/04 C
27/10 325 J

[Procedure amendment]
[Filing Date] October 6, Heisei 12 (2000. 10.6)
[Procedure amendment 1]
[Document to be Amended] Description
[Item(s) to be Amended] Claim
[Method of Amendment] Modification
[Proposed Amendment]
[Claim(s)]
[Claim 1] A semiconductor substrate,
A ferroelectric thin film capacitor which covers said semiconductor substrate formed on said semiconductor substrate which consists of an oxide ferroelectric layer prepared between two an electrode layer and this electrode layer,
Ferroelectric random-access memory characterized by providing a protective coat which covers said ferroelectric thin film capacitor which prevents diffusion of hydrogen to said oxide ferroelectric layer.
[Claim 2] Ferroelectric random-access memory according to claim 1 characterized by including the same oxide as an oxide which said oxide ferroelectric layer from which said protective coat constitutes said ferroelectric thin film capacitor contains.
[Claim 3] Ferroelectric random-access memory according to claim 1 characterized by including an oxide containing the same element as an element which said oxide ferroelectric layer from which said protective coat constitutes said ferroelectric thin film capacitor contains.
[Claim 4] Ferroelectric random-access memory according to claim 1 characterized by preparing a protective coat and an undercoating layer of this presentation and this structure between said semiconductor substrates and ferroelectric capacitors.
[Claim 5] Ferroelectric random-access memory according to claim 1 characterized by for the transistor elements separately prepared on said ferroelectric thin film capacitor and semiconductor substrate separating an interlayer insulation film by which the laminating was carried out to said protective coat and/or this protective coat, and connecting them to them electrically with a laminating wiring electrode of alumimium nitride and an aluminum-silicon alloy.
[Claim 6] Ferroelectric random-access memory according to claim 1 characterized by for said oxide ferroelectric thin film consisting of a bismuth stratified perovskite mold compound which has a presentation expressed by the following general formula (1), and having a concentration gradient of the following element B in the direction of thickness, and an element B containing richly in an interface with an up electrode.
(Bi2O2)2+(Am-1BmO3m+1)2-
However, be based on one or an arbitration ratio which consists of base chosen from from among A=Bi, and Pb, Ba, Sr, calcium, Na, K and Cd, and combine with it. Be based on one or an arbitration ratio which consists of base chosen from from among B=Ti, and Nb, Ta, W, Mo, Fe, Co and Cr, and combine with it. The natural number of m=1-5.
[Claim 7] Ferroelectric random-access memory according to claim 6 characterized by for said bismuth stratified perovskite compound being SrBi2(TaXNb1-X)2O9 (x=0-1.0), and an element B being Ta or Nb.
[Claim 8] Ferroelectric random-access memory according to claim 1 characterized by said protective coat using aluminum, silicon, or a nitride thin film of titanium as main components.

[Claim 9] Ferroelectric random-access memory according to claim 2 to which said protective coat is characterized by being a partial crystal film.
[Claim 10] Ferroelectric random-access memory according to claim 2 to which said protective coat is characterized by being an amorphous film.
[Procedure amendment 2]
[Document to be Amended] Description
[Item(s) to be Amended] 0013
[Method of Amendment] Modification
[Proposed Amendment]
[0013]
[Means for Solving the Problem] This invention is ferroelectric random-access memory characterized by providing a ferroelectric thin film capacitor which consists of an oxide ferroelectric layer prepared between two electrode layers which are prepared on a semiconductor substrate and this substrate and cover the above-mentioned substrate, and this electrode layer, and a protective coat which prevents diffusion of hydrogen to an oxide ferroelectric layer which covers this ferroelectric thin film capacitor.

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3-1 ②

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報**（Ａ）　(11)特許出願公開番号

特開平7－111318

(43)公開日　平成７年(1995)４月25日

(51)Int.Cl.[6]	識別記号	庁内整理番号	ＦＩ		技術表示箇所
Ｈ０１Ｌ　27/10	４５１	7210－4M			
Ｇ１１Ｃ　11/22					
Ｈ０１Ｌ　27/04					
		8832－4M	Ｈ０１Ｌ　27/ 04		Ｃ
		7210－4M	27/ 10	３２５	Ｊ

審査請求　未請求　請求項の数７　ＯＬ　（全 10 頁）　最終頁に続く

(21)出願番号　特願平5－254378

(22)出願日　平成５年(1993)10月12日

(71)出願人　000000376
オリンパス光学工業株式会社
東京都渋谷区幡ヶ谷２丁目43番２号

(71)出願人　590006468
シメトリックス・コーポレーション
ＳＹＭＥＴＲＩＸ　ＣＯＲＰＯＲＡＴＩＯＮ
アメリカ合衆国、コロラド州　80918、コロラド・スプリングス、ナンバー100、マーク・ダブリング・ブールバード　5055

(74)代理人　弁理士　鈴江　武彦

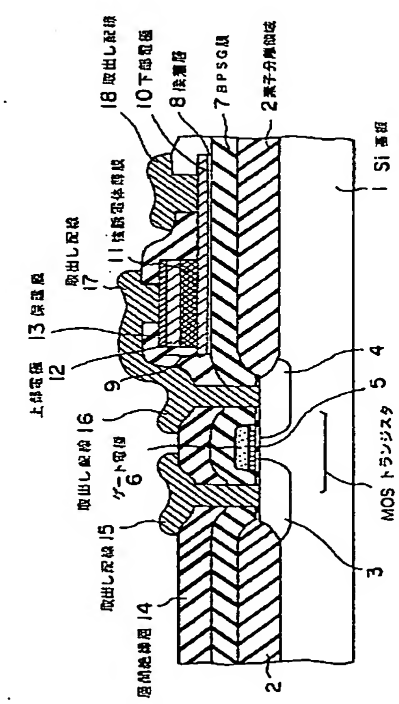
最終頁に続く

(54)【発明の名称】　強誘電体メモリ

(57)【要約】

【目的】この発明は、酸化物強誘電体表面の還元反応、変質を阻止するとともに、ＭＯＳシンター工程において強誘電体薄膜と上下電極間の剥離を防止することを主要な目的とする。

【構成】半導体基板(1) と、この基板(1) 上に設けられ、下部電極(10)，酸化物強誘電体薄膜(11)，上部電極(12)の順次積層して構成される誘電体薄膜キャパシタ(9) と、このキャパシタ(9) 表面に被覆された、アルミニウム，シリコンもしくはチタンの窒化物薄膜を主要な構成要素とする保護膜(12)とを具備したことを特徴とする強誘電体メモリ。



【特許請求の範囲】

【請求項1】　半導体基板と、この基板上に設けられ、下部電極，酸化物強誘電体薄膜，上部電極の順次積層して構成される強誘電体薄膜キャパシタと、このキャパシタ表面に被覆された、アルミニウム，シリコンもしくはチタンの窒化物薄膜を主要な構成要素とする保護膜とを具備したことを特徴とする強誘電体メモリ。

【請求項2】　前記保護膜が、強誘電体薄膜キャパシタを構成する酸化物強誘電体と同組成または一部構成元素を共有する酸化物薄膜を主要な構成要素とするものであることを特徴とする請求項記載の強誘電体メモリ。

【請求項3】　前記保護膜が、部分結晶膜又は非晶質膜であることを特徴とする請求項1記載の強誘電体メモリ。

【請求項4】　前記半導体基板と強誘電体薄膜キャパシタ間に保護膜と同組成、同構造の下引層を設けたことを特徴とする請求項1記載の強誘電体メモリ。

【請求項5】　前記強誘電体薄膜キャパシタと半導体基板上に別途設けられたトランジスタ素子群が前記保護膜及び／又はこの保護膜に積層された層間絶縁膜を隔てて窒化アルミニウムとアルミニウム－シリコン合金の積層配線電極で電気的に接続されていることを特徴とする請求項1記載の強誘電体メモリ。

【請求項6】　前記酸化物強強誘電体薄膜が、下記一般式（1）で表現される組成を有するビスマス層状ペロブスカイト型化合物からなり、かつ膜厚方向に下記元素Bの濃度勾配を有し、上部電極との界面においては元素Bが富裕に含有されていることを特徴とする請求項1記載の強誘電体メモリ。

$$(Bi_2O_2)^{2+}(A_{m-1}B_mO_{3m+1})^{2-} \quad \cdots(1)$$

但し、A＝Bi、Pb、Ba、Sr、Ca、Na、K、Cdの内から選ばれる1つもしくは複数元素からなる任意比率による組み合わせ。B＝Ti、Nb、Ta、W、Mo、Fe、Co、Crの内から選ばれる1つもしくは複数元素からなる任意比率による組み合わせ。m＝1～5の自然数。

【請求項7】　前記ビスマス層状ペロブスカイト型化合物が$SrBi_2(Ta_xNb_{1-x})_2O_9$（x＝0～1．0）であり、元素BがTa又はNbであることを特徴とする請求項1記載の強誘電体メモリ。

【発明の詳細な説明】

【0001】

【産業上の利用分野】この発明は強誘電体メモリに関し、特に酸化物強誘電体薄膜の残留分極特性を利用した強誘電体メモリに関する。

【0002】

【従来の技術】従来、強誘電体化合物は、その特異な電気特性を利用して多くの分野に応用されている。例えば、圧電性を利用した圧電フィルタや超音波トランスデューサに、また焦電性を利用して赤外線センサやパイロビジコンに、あるいは電気光学効果を利用した光変調素子や光シャッタ等の多方面に応用されている。さらにこれらの材料の薄膜を利用した電子デバイスも考案され、薄膜化の検討が精力的になされている。特に、残留分極の安定性を利用した強誘電体薄膜キャパシタ搭載の不揮発性メモリデバイスは、最近の記憶容量の高密度化、高集積化競争を背景にもっとも注目されている分野である。

【0003】こうした多用途に応じて競って研究されてる代表材料として、PZT（チタン酸ジルコン酸鉛）、PLZT（チタン酸ジルコン酸ランタン鉛）等、一連の鉛含有複合酸化物強誘電体が挙げられ、多年にわたって多くの研究者により実用化の検討が続けられている。

【0004】また、その他の有望誘電体材料として、ビスマス層状ペロブスカイト型酸化物強誘電体の薄膜も従来の中心材料であったPZT，PLZT等の薄膜に比較して情報の記録消去回数でさらに数桁以上上回る優れた耐疲労特性を示し、高い耐久性能を有する不揮発性メモリデバイス、その他の電子、光学デバイスに応用することができる。

【0005】上記の強誘電体薄膜は、予め焼成したセラミックターゲットを用いたスパッタ法や金属の反応蒸着法等の物理的成膜法、金属有機化合物を気相堆積するCVD法、同様の化合物溶液を塗布することによって成膜するゾルゲル法、MOD法等によって形成することができる。

【0006】一般に、強誘電体材料は残留分極のヒステリシス特性を有し、この特性を利用して不揮発性メモリとしてデータを記憶することができる。こうした強誘電体材料を用いた強誘電体メモリ1は、図1に示すように、MOSトランジスタ等で構成されるスイッチング素子、増幅アンプ等の周辺素子群2を形成した例えばシリコン半導体からなる基板3上に、白金等を用いた下部電極4、強誘電体薄膜5、上部電極6を順次積層してなる強誘電体薄膜キャパシタ7を設け、更にスパッタ法やCVD法によりシリコン酸化膜からなる層間絶縁膜8を設け、更には配線電極9により素子間を接続して構成される。

【0007】以上の基本構造に加えて、下部電極4の基板密着性を向上させるための下引き層10や強誘電体薄膜キャパシタを各種環境変化から保護するための保護膜（図示せず）等が必要に応じて設けられる。ここで、従来の強誘電体メモリの保護膜としては、例えば下記のものが提案されている。

(1) 強誘電体PZT薄膜と上部電極間にTi_3N_4層を設けると同時にPZTを直接Si_3N_4層で被覆することによってPZTからの酸素脱離を防ぎ、スイッチング疲労特性を改善する（特開平2－183569号）。

(2) 白金又はパラジウムからなる第１導電膜とチタン，窒化チタン，チタン－タングステン合金，モリブデンシリサイドからなる第２導電膜を積層してキャパシタ上部電極とすることによりアルミニウム配線電極と第１導電層の合金化を防止して後工程における熱処理を可能とする（特開平２－９０６０６号）。

【０００８】

【発明が解決しようとする課題】しかしながら、前述した強誘電体メモリは、その製造過程においてスパッタ法やスピオン法で成膜された強誘電体薄膜の結晶化に不可欠な６００～９００℃に及ぶ比較的高温の熱処理工程を経たり、イオンミリング等の高エネルギービームによる加工工程や反応性プラズマエッチングによるプラズマ被爆によって、半導体シリコン基板の単結晶構造中に多数の格子欠陥を生じ、これが基板上のＭＯＳトランジスター特性を劣化させる。

【０００９】このため、特性改善のために最終工程において水素混合窒素ガス（フォーミングガス）雰囲気中において３５０～４５０℃の熱処理（ＭＯＳシンター）を行なうことにより、H_2 の還元性を利用して単結晶シリコン中に発生したダングリングボンド等の欠点を終端し劣化したＭＯＳ特性を修復する必要がある。

【００１０】ところが、強誘電体薄膜用電極材料として水素に対して易透過性である白金等が使用される。そのため、還元性雰囲気中の熱処理工程において、上記層間絶縁膜及び上部電極を拡散通過して上部電極と強誘電体薄膜の界面及びキャパシタ側面まで到達した水素の還元作用によって、界面近傍の酸化物が酸化還元反応を起こしたり分解して、この界面における化学変化に起因して上部電極との密着性が低下したり、反応生成物である酸素、水等によって上部電極が押し上げられたりして、その結果上部電極と強誘電体薄膜との界面で剥離を発生させる問題があった。

【００１１】また、時には還元性雰囲気のデバイス内部への浸透はキャパシタ側面を通して下部電極まで及ぶと考えられ、比較的大きな内部応力が残留し易いＡｌ－Ｓｉ配線電極を用いた場合にはキャパシタ全体が半導体基板そのものから剥離してしまうような不具合も生じることがあった。このような問題は、強誘電体薄膜キャパシタとシリコン半導体デバイスを組み合わせて強誘電体メモリを構成する上で新たな対策が必要とされてきた。

【００１２】この発明はこうした事情を考慮してなされたもので、酸化物強誘電体薄膜キャパシタとシリコンデバイスとで構成される強誘電体メモリにおいて還元性雰囲気下でのＭＯＳシンター工程において強誘電体薄膜と上下電極間の剥離を防止しえる構造を提供することを目的とする。

【００１３】

【課題を解決するための手段】この発明は、半導体基板と、この基板上に設けられ、下部電極，酸化物強誘電体

薄膜，上部電極の順次積層して構成される強誘電体薄膜キャパシタと、このキャパシタ表面に被覆された、アルミニウム，シリコンもしくはチタンの窒化物薄膜を主要な構成要素とする保護膜とを具備したことを特徴とする強誘電体メモリである。

【００１４】この発明において、前記保護膜の材料であるアルミニウム，シリコンもしくはチタンの窒化物薄膜は、膜密度が比較的高く、酸化物と比較して化学的にも安定であり容易には水素ガスを透過させず、膜厚は２０ｎｍ～１００ｎｍの範囲にすることが望ましい。

【００１５】前記窒化物薄膜は、周知の各種成膜法、例えばｄｃ又はｒｆスパッタ法やイオンビームデポジション、ＣＶＤ法、時にはゾルゲル法を用いることで容易に成膜可能である。

【００１６】この発明において、主要な構成要素とは還元性ガスの拡散透過を防止する効果を指しており、他の構成要素としては前記窒化物薄膜と上部電極又は層間絶縁膜との密着性を改善するために設けられる補強層などのことをいう。通常、窒化物薄膜と他の薄膜とを積層する場合の補強層としては、共有金属の酸化物薄膜が適している。特に、酸化物補強層の存在によって窒化物薄膜の電極剥離防止効果が損なわれることはない。

【００１７】なお、上記窒化物のうちチタン、アルミニウムの窒化物は導電性を維持できるため、キャパシタ上部電極の全面を被覆して水素遮蔽効果を上げることができる。窒化シリコンの場合は絶縁性であるため、配線電極と上部電極を電気的に接合するためのコンタクトホールを穿って貫通させる必要がある。従って、コンタクトホールの面積分だけ保護膜が除去されるため、保護膜としての効果は低下するがキャパシタ側面を直接被覆できるため、側方への回り込みを防止できる。また、１種類の保護膜でキャパシタを保護するのではなく、上部電極面をアルミニウムもしくはチタンの窒化物、側面をシリコン窒化物で併用被覆してもよい。

【００１８】この発明において、上記金属窒化物薄膜以外の保護膜として、保護される対象である強誘電体薄膜キャパシタを構成する強誘電体材料と同組成又は一部構成元素を共有する酸化物強誘電体薄膜で上部電極表面を被覆することも有効な手段である。配線電極，層間絶縁膜を拡散透過して上部電極上に設けられたこの酸化物強誘電体からなる保護膜表面まで到達した水素は酸化物強誘電体の還元反応に消費され上部電極を越えて内部まで到達することがない。

【００１９】従って、この場合の保護膜材料として最も好ましいのは組成的にも結晶構造の上でも同等であり、水素との反応性もキャパシタ強誘電体薄膜と等しい薄膜である。但し、メモリデバイスの構造上数種の電極や金属層がこれを挟んで存在するような場合は、保護膜が単なる誘電体でなく強誘電体であるとデバイスの動作そのものに支障をきたすこともある。そのような場合は、保

護膜成膜時の焼成温度を強誘電体の結晶化温度以下にすることにより非晶質もしくは部分結晶化するに止め、強誘電性の発現を抑制することが望ましい。

【0020】このように自ら還元性気体と反応することによって、それ以上の内部拡散を抑止する効果を示す薄膜材料は、必ずしも強誘電体薄膜キャパシタを構成する酸化物強誘電体と同一組成ではなくともよく、例えば一部元素を置き換えた化合物や特定元素を取り除いた化合物も同じ目的に供し得る。例えば、$SrBi_2Ta_2O_9$ 薄膜をキャパシタ材料とするデバイスでは $SrTa_2O_6$ や $SrBi_2Nb_2O_9$ の薄膜も保護膜として十分な効果を与える。このときもこれらの保護膜は充分酸化されていれば結晶化膜であっても、部分結晶化膜であっても、さらには非晶質膜であってもよいのは当然である。

【0021】更には、上記保護膜は強誘電体キャパシタ上部電極の外表面だけでなく、キャパシタ群を直接被覆する層間絶縁膜の上から（配線電極の下引き層として）基板全体を被覆する構成をとっても同様の効果を与えることができる。加えて、この保護膜と同組成、同構造の下引き層をシリコン基板表面に設けその上にキャパシタ下部電極を形成し、上述の構造にしたがって、強誘電体メモリを構成してもよい。この下引き層はキャパシタ側面から回り込む還元性気体を遮蔽し、下部電極からの剥離を防止する効果を示す。

【0022】また、当然の構成として配線電極まで構成した強誘電体メモリの表面全面を本発明の保護膜を用いて被覆することによっても強誘電体薄膜キャパシタへの還元気体の影響を防止することができる。この場合、保護膜は多層膜であってもよく、例えば酸化シリコン膜を介して設けるも、逆の構成として保護膜の表面にさらに同様の酸化シリコンの層を設けてもよい。この構成においては保護膜による水素透過防止効果が大き過ぎて、MOSトランジスタ部へ特性回復に十分な水素量を供給できないため、MOSトランジスタ部上の保護膜を除去した構成することもできる。

【0023】上述の電極剥離防止の保護膜を含む強誘電体メモリの構造は強誘電体材料の種類を選ばないが、酸化物強誘電体薄膜が下記の一般式（1）で表現される組成を有するビスマス層状ペロブスカイト型化合物からなる場合は、強誘電体材料の組成そのものを調整することによっても著しい剥離防止効果を得ることができる。式（1）におけるBサイト元素は金属状態であっても、また酸化物状態にあってもそのいずれもが酸化シリコンやその他の金属との密着性に優れ電極金属や下引き層や熱膨脹率、格子定数の異なる層間の接合層として多用される元素である。

【0024】ここで、強誘電体薄膜の成膜時に、予めB元素過剰に成膜し、高温で焼成することによって化学量論組成の膜と同様の強誘電体相と過剰配合によって、その多くは薄膜表面に、偏析した元素Bの酸化物微粒子を同時に形成することができる。同様の元素Bの表面偏析は下層に化学量論比組成、上層に元素B過剰組成の多層膜を形成してこれを焼成しても実現することができる。

【0025】

$$(Bi_2O_2)^{2+}(A_{m-1}B_mO_{3m+1})^{2-} \quad \cdots (1)$$

但し、A＝Bi、Pb、Ba、Sr、Ca、Na、K、Cdの内から選ばれる1つもしくは複数元素からなる任意比率による組み合わせ。B＝Ti、Nb、Ta、W、Mo、Fe、Co、Crの内から選ばれる1つもしくは複数元素からなる任意比率による組み合わせ。

【0026】m＝1～5の自然数。こうして得られた膜厚方向に元素Bの濃度勾配を有し、上部電極との界面においては元素Bが富裕に含有されているビスマス層状ペロブスカイト型化合物からなる強誘電体薄膜で構成された薄膜キャパシタでは、還元性雰囲気中でのフォーミング処理において、一部の結晶構造は還元されて破壊されて若干の残留分極量低下と抗電界の増加が見られるが、偏析成分であるところのB元素酸化物もしくはその一部還元体が電極金属との接合を合金化反応をも含んで補強することによって、電極の剥離を防止する効果を発生する。特に、キャパシタ強誘電体が $SrBi_2(Ta_xNb_{1-x})_2O_9$ （x＝0～1.0）で表されるビスマス層状ペロブスカイト型化合物であり、元素BがTaまたはNbである場合は残留分極量の絶対値並びに電極接合強度共に優れた強誘電体メモリを構成することができる。

【0027】

【作用】この発明によれば、強誘電体薄膜キャパシタの上部電極の表面やキャパシタ側面等に還元性ガスの内部拡散浸透を防止する保護膜を設けること、又は、強誘電体材料薄膜の一部構成元素を過剰に配合することにより、酸化物強誘電体表面の還元反応、変質を阻止できる。また、従来のようにフォーミング処理により上部電極，下部電極が強誘電体薄膜から剥離するのを防止できる。

【0028】

【実施例】以下、本発明の実施例を比較例とともに図面を参照して説明する。

（実施例1）図1を参照する。図中の1は、表面に素子分離領域2が形成されたシリコン基板である。前記素子分離領域2で囲まれた基板1の素子領域にはソース領域3，ドレイン領域4が形成され、更にこれら領域3，4間の基板1上にはゲート絶縁膜5を介してゲート電極6が形成されている。ここで、前記ソース・ドレイン領域3，4及びゲート電極6を総称してMOSトランジスタと呼ぶ。

【0029】前記素子分離領域2を含む基板1全面に

は、ＢＰＳＧ（ボロン燐ドープ酸化シリコン）膜７が形成されている。前記素子分離領域２上のＢＰＳＧ膜７上には、チタン等の膜厚２０ｎｍの下引層（接着層）８を介して強誘電体薄膜キャパシタ９が形成されている。この強誘電体薄膜キャパシタ９は、Ｐｔからなる膜厚２００ｎｍの下部電極10と、この下部電極10上に順次形成された強誘電体薄膜11及びＰｔからなる膜厚２００ｎｍの上部電極12から形成され、上部電極12上には膜厚５０ｎｍの保護膜13とから構成されている。前記強誘電体薄膜11は、ＰＺＴ（40／60）のゾルゲル薄膜からなる。

【００３０】前記強誘電体薄膜キャパシタ９を含む前記ＢＰＳＧ膜７上には、層間絶縁膜14が形成されている。前記ＭＯＳトランジスタのソース領域３，ドレイン領域に対応する前記層間絶縁膜14及びＢＰＳＧ膜７には開口部が形成され、この開口部にソース取出し配線15，ドレイン取出し配線16が形成されている。また、前記強誘電体薄膜キャパシタ９の上部保護膜13，下部電極10に対応する前記層間絶縁膜14にも開口部が形成され、これら開口部に上部電極用取出し配線17，下部電極用取出し配線18が形成されている。前記ドレイン取出し配線16と上部電極用取出し配線17とは電気的に接続されている。また、上記各取出し配線はＡｌ－Ｓｉからなる。

【００３１】図１の構成の強誘電体メモリは次のようにして製造する。

(1) まず、半導体微細加工技術等の周知の技術により、基板１の表面に素子分離領域２を形成した後、この素子分離領域２で囲まれた素子領域にソース領域３，ドレイン領域４，ゲート電極６などからなるＭＯＳトランジスタを形成した。つづいて、基板全面にＢＰＳＧ膜７を形成したたの後、前記素子分離領域２上にｄｃスパッタ法により膜厚２００ｎｍの下部電極10を、膜厚２０ｎｍの接着層８を介して形成した。次に、所定の濃度、組成に調整、部分加水分解を施したゾルゲルＰＺＴ前駆体溶液のスピンコート塗布、乾燥、仮焼を繰り返して所望膜厚の仮焼薄膜を成膜し、最後に酸素雰囲気中で所定の温度において焼成処理を行って膜厚３００ｎｍの強誘電性ＰＺＴ薄膜（強誘電体薄膜）11を得た。ひきつづき、前記強誘電体薄膜11上に下部電極10と同膜厚（２００ｎｍ）の上部電極材をスパッタし、更に上部電極10上にｄｃスパッタで膜厚５０ｎｍの窒化アルミニウム（ＡｌＮ）からなる保護膜13を成膜した後、各電極，強誘電体薄膜11の加工をイオンミリングにて行ない強誘電体薄膜キャパシタ９を形成した。

【００３２】(2) 次に、全面にスピンオンガラスをスピンコートし、所定の工程に従って乾燥、焼成を行ない、膜厚４００ｎｍの層間絶縁膜14を形成した。つづいて、前記ＭＯＳトランジスタのソース領域３，ドレイン領域４に対応する前記層間絶縁膜14及びＢＰＳＧ膜７、及び強誘電体薄膜キャパシタ９の保護膜13，下部電極10に対応する層間絶縁膜14に夫々コンタクトホールを形成した。更に、全面にスパッタ法によりＡｌ－Ｓｉからなる膜厚３００ｎｍの配線材料膜を成膜し、周知のウェットエッチ法を用いてこの配線材料膜をパターニングし、前記各コンタクトホールにソース取出し配線15，ドレイン取出し配線16，上部電極用取出し配線17，下部電極用取出し配線18が形成し、強誘電体薄膜キャパシタとＭＯＳトランジスタが電気的に接続された強誘電体メモリを製造した。

【００３３】このように、実施例１の強誘電体メモリは、互いに電気的に接続されたＭＯＳトランジスタ６と強誘電体薄膜キャパシタ９からなり、前記ＭＯＳトランジスタ６は素子領域に形成されたソース領域３，ドレイン領域４及びゲート電極６などから構成され、前記強誘電体薄膜キャパシタ９は素子分離領域２上のＢＰＳＧ膜７上に接着層８を介して形成された下部電極10，強誘電性ＰＺＴ薄膜（強誘電体薄膜）11及び上部電極12から構成されている。しかるに、前記キャパシタ９の上面特に上部電極12の上面はＡｌＮからなる保護膜13で被覆された構成されているため、還元性ガスの内部透過を遮断でき、強誘電体薄膜11表面の還元反応とこれに起因する電極剥離を防止することができる。

【００３４】（実施例２）この実施例２は、実施例１と比べ、膜厚５０ｎｍの窒化チタン（Ti_3N_4）からなる保護膜を用いた点を除いて、全く同様な構成である。窒化チタンからなる保護膜を用いた実施例２に係る強誘電体メモリによれば、実施例１と同様な効果が得られる。

【００３５】（実施例３）図２を参照する。但し、図１と同部材は同符号を付して説明は省略する。図中の21は、強誘電体薄膜キャパシタ９の上面のみならず側面にも被覆形成された窒化シリコン（Si_3N_4）からなる膜厚５０ｎｍの保護膜である。この保護膜21は、強誘電体薄膜キャパシタ９を形成した後、全面にｄｃスパッタで窒化シリコンを成膜することにより形成する。

【００３６】上記実施例３によれば、強誘電体薄膜キャパシタ９の上面のみならず側面にも窒化シリコンからなる保護膜21が形成されているため、還元性ガスのキャパシタ側方への廻り込みを防止できる。

【００３７】（実施例４）図３を参照する。但し、図１，３と同部材は同符号を付して説明は省略する。この実施例４は、強誘電体薄膜キャパシタ９の上面のみに形成されたＡｌＮからなる保護膜13と、前記保護膜13の一部及び強誘電体薄膜キャパシタ９の側面を被覆する窒化シリコンからなる保護膜21を組み合わせた構成であることが特徴である。上記実施例４によれば、２種類の保護膜13，21の組み合わせにより強誘電体薄膜キャパシタ９の上部電極12の上面を被覆して水素遮蔽効果を上げることができるほか、還元性ガスのキャパシタ側方への廻り込みを防止できる。

【００３８】（実施例５）この実施例５は、実施例３と

比べ、膜厚５０ｎｍの酸化シリコン（SiO_2）からなる保護膜と、この保護膜上の膜厚５０ｎｍの窒化シリコン（Si_3N_4）からなる保護膜の２層構造とした点を除いて、他の構成は全く同じである。

【００３９】（実施例６）図４を参照する。但し、図１と同部材は同符号を付して説明は省略する。この実施例６は、実施例１と比べ、図１に図示されたＡｌＮからなる保護膜13の他に、コンタクトホール周辺の層間絶縁膜14上にもＡｌＮからなる保護膜41を設けた点が異なる。上記実施例６によれば、保護膜13を強誘電体薄膜キャパシタ９の上部電極12の上面に被覆するのみならず、キャパシタ群を直接被覆する層間絶縁膜14の上から基板全体を被覆するため、上部電極への水素遮蔽効果を上げることができるほか、還元性ガスのキャパシタ側方への廻り込みを防止できる。

【００４０】（実施例７）図５を参照する。但し、図１と同部材は同符号を付して説明を省略する。この実施例７は、実施例１と比べ、ＢＰＳＧ膜７と接着層８間にＡｌＮからなる膜厚５０ｎｍの保護膜51を設けた点を除いて全く同様な構成になっている。ここで、前記保護膜51，接着層８及び下部電極10は１つのマスクで同時にパターニングにより形成してもよいし、別工程で形成してもよい。

【００４１】（実施例８）この実施例８は、実施例３と比べ、強誘電体薄膜キャパシタの強誘電体薄膜として、ビスマス層状ペロブスカイト型化合物$SrBi_2Ta_2O_9$のＭＯＤ薄膜（膜厚２５０ｎｍ）を用いる点、及び保護膜として膜厚８０ｎｍの強誘電性$SrBi_2Ta_2O_9$薄膜を用いる点が異なる。ここで、前記保護膜は、$SrBi_2Ta_2O_9$のＭＯＤ前駆体溶液を１層スピンコート塗布し、乾燥、仮焼を行なって仮焼薄膜を成膜し、次いで酸素雰囲気中で８００℃において焼成処理を行なうことにより得た。

【００４２】（実施例９）この実施例９は、実施例３と比べ、強誘電体薄膜キャパシタの強誘電体薄膜として、ビスマス層状ペロブスカイト型化合物$SrBi_2Ta_2O_9$のＭＯＤ薄膜（膜厚２５０ｎｍ）を用いる点、及び保護膜として膜厚８０ｎｍの非強誘電性酸化物の非晶質膜を用いる点が異なる。ここで、前記保護膜は、$SrBi_2Ta_2O_9$のＭＯＤ前駆体溶液を１層スピンコート塗布し、乾燥、４００℃仮焼を行なって仮焼薄膜を成膜し、ひきつづき酸素雰囲気中で上記化合物の結晶化温度よりも十分低い６００℃において焼成処理を行なって十分焼き締めることにより得た。

【００４３】（実施例１０）この実施例１０は、実施例３と比べ、強誘電体薄膜キャパシタの強誘電体薄膜として、ビスマス層状ペロブスカイト型化合物$SrBi_2Ta_2O_9$のＭＯＤ薄膜（膜厚２５０ｎｍ）を用いる点、及び保護膜として膜厚８０ｎｍの結晶性薄膜を用いる点が異なる。ここで、前記結晶性薄膜は、薄膜キャパシタの強誘電体$SrBi_2Ta_2O_9$と一部共通の元素で構成される$SrTa_2O_6$（タンタル酸ストロンチウム）のＭＯＤ前駆体溶液を１層スピンコート塗布し、乾燥、４００℃仮焼を行なって仮焼薄膜を成膜し、ひきつづき酸素雰囲気中で８００℃において焼成処理を行なうことにより得た。

【００４４】（実施例１１）この実施例１１は、実施例３と比べ、強誘電体薄膜キャパシタの強誘電体薄膜として、ビスマス層状ペロブスカイト型化合物$SrBi_2Ta_2O_9$のＭＯＤ薄膜（膜厚２５０ｎｍ）を用いる点、及び保護膜として膜厚８０ｎｍの強誘電体性の$SrBi_2Nb_2O_9$薄膜を用いる点が異なる。ここで、前記強誘電体性薄膜は、$SrBi_2Nb_2O_9$の組成を有するＭＯＤ前駆体溶液を１層スピンコート塗布し、乾燥、仮焼をを行なって仮焼薄膜を成膜し、ひきつづき酸素雰囲気中で８５０℃において焼成処理を行なうことにより得た。

【００４５】（実施例１２）図６を参照する。但し、図１及び図５と同部材は同符号を付して説明を省略する。この実施例12は、実施例１と比べ、ＢＰＳＧ膜７の表面に保護膜としての膜厚８０ｎｍの強誘電体性$SrBi_2Ta_2O_9$薄膜61を用いるとともに、キャパシタの上部電極12上に膜厚１００ｎｍの強誘電体性$SrBi_2Ta_2O_9$薄膜62を設けた点を除いて全く同様な構成になっている。ここで、前記薄膜61は、$SrBi_2Ta_2O_9$の前駆体溶液を１層スピンコート塗布し、乾燥、仮焼をを行なって仮焼薄膜を成膜し、ひきつづき酸素雰囲気中で８００℃において焼成処理を行なうことにより得た。また、前記薄膜62も、薄膜61と同様、$SrBi_2Ta_2O_9$の前駆体溶液を１層スピンコート塗布し、乾燥、仮焼を行なって仮焼薄膜を成膜し、ひきつづき酸素雰囲気中で８００℃において焼成処理を行なうことにより得た。

【００４６】（実施例１３）この実施例13は、実施例１と比べ、上部電極に保護膜を設けない点、及び強誘電体薄膜としてタンタル過剰強誘電性$SrBi_2Ta_2O_9$薄膜を用いた点を除いて、構造が同じである。ここで、前記薄膜は次のようにして得られる。即ち、下部電極を形成した後、$SrBi_2Ta_2O_9$の前駆体溶液を化学量論比に対してタンタルが２０モル％過剰となるように塗布溶液を調整して、スピンコート塗布し、乾燥、仮焼を繰り返して仮焼薄膜を成膜し、ひきつづき酸素雰囲気中で８００℃において焼成処理を行なうことにより得た。このようにして得られた前記薄膜をＸ線回折、ＩＣＰ分析、電子顕微鏡観察等によって結晶構造を解析し、薄膜組成分析を行なったところ、薄膜内部では強誘電相と酸化タンタルを主とする常誘電相が混在し、薄膜表面には酸化タンタルが多く偏析していることが確認された。

【００４７】（実施例１４）この実施例14は、実施例13

と強誘電体薄膜のみが異なる。ここで、この強誘電体薄膜は、次のようにして得られる。即ち、下部電極を形成した後、$SrBi_2Ta_2O_9$ の前駆体の化学量論比溶液をスピンコート塗布し、乾燥、仮焼のサイクルを２回繰り返して仮焼薄膜を成膜し、最終層に化学量論比に対してタンタルが２０モル％過剰となるように調整した第２の前駆体溶液を塗布、乾燥、仮焼して仮焼薄膜を成膜し、ひきつづき酸素雰囲気中で８００℃において焼成処理を行なうことにより得た。このようにして得られた前記薄膜をX線回折、ＩＣＰ分析、電子顕微鏡観察等によって結晶構造を解析し、薄膜組成分析を行なったところ、薄膜の大部分は強誘電相の $SrBi_2Ta_2O_9$ であり、薄膜表面にのみ酸化タンタルの偏析が確認された。

（比較例１）図７を参照する。但し、図１と同部材は同符号を付して説明を省略する。比較例１は、図１と比べ、保護膜を設けていない点を除いて、全く同じ構成となっている。但し、強誘電体として膜厚３００ｎｍの $Pb(Zr_{0.4}Ti_{0.6})O_3$ 薄膜を用いた。

【００４８】（比較例２）比較例２は、図１と比べ、保護膜を設けていない点を除いて、全く同じ構成となっている。但し、強誘電体として膜厚３００ｎｍの $SrBi_2Ta_2O_9$ 薄膜を用いた。

【００４９】（実施例１５）比較例２（$SrBi_2Ta_2O_9$ 薄膜を用いた強誘電体メモリ、配線電極パターン形成済み）上に、薄膜キャパシタ強誘電体を形成した $SrBi_2Ta_2O_9$ 薄膜を成膜し、次いで酸素雰囲気中で６００℃において焼成処理を行なって、膜厚１００ｎｍの非結晶性、非誘電性の $SrBi_2Ta_2O_9$ 薄膜で表面被覆した。この後、この保護膜にMOSトランジスタ部に対応する部分のみ配線電極を露出させたMOSコンタクトホールを開口し、図８の強誘電体メモリを得た。なお、図８において、81はコンタクトホール、83は保護膜を示す。

【００５０】上記実施例及び比較例１，２に係る強誘電体メモリを拡散炉中で水素５％を含む窒素ガス（フォーミグガス）雰囲気にて４２５℃、３０分間のMOSシンター処理を行なった。その結果、比較例１，２では強誘電体薄膜－上部電極界面ではほとんどのキャパシタが剥離を起こした。これに対し、全ての実施例では電極剥離

が観察されず、強誘電ヒステリシス特性もMOSトランジスタ特性も良好で、強誘電体メモリは完全に動作した。

【００５１】なお、上記各実施例では、下部電極，強誘電体薄膜，上部電極，保護膜，取出し配線等の材料の一例を述べたが、これらの材料に限定されないことは勿論のことである。

【００５２】

【発明の効果】以上詳述したようにこの発明によれば、還元性ガスの内部拡散浸透を防止する保護膜を設けること、又は、強誘電体材料膜の一部構成元素を過剰に配合することにより、酸化物強誘電体表面の還元反応、変質を阻止し、また従来のようにMOSシンター工程において強誘電体薄膜と上下電極間の剥離を防止して、実用に供し得る強誘電体メモリを提供できる。

【図面の簡単な説明】

【図１】この発明の実施例１に係る強誘電体メモリの断面図。

【図２】この発明の実施例３に係る強誘電体メモリの断面図。

【図３】この発明の実施例４に係る強誘電体メモリの断面図。

【図４】この発明の実施例６に係る強誘電体メモリの断面図。

【図５】この発明の実施例７に係る強誘電体メモリの断面図。

【図６】この発明の実施例12に係る強誘電体メモリの断面図。

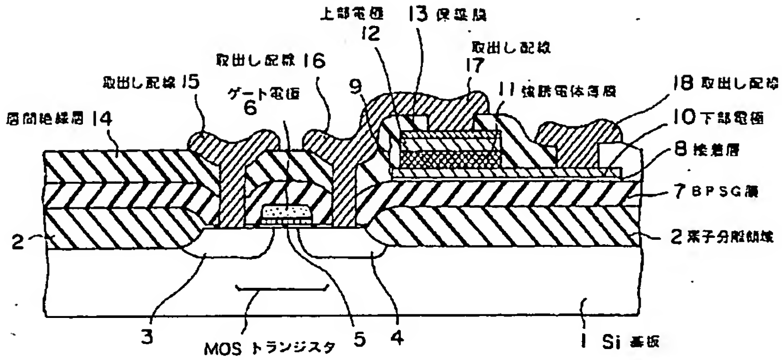
【図７】比較例１に係る強誘電体メモリの断面図。

【図８】この発明の実施例15に係る強誘電体メモリの断面図。

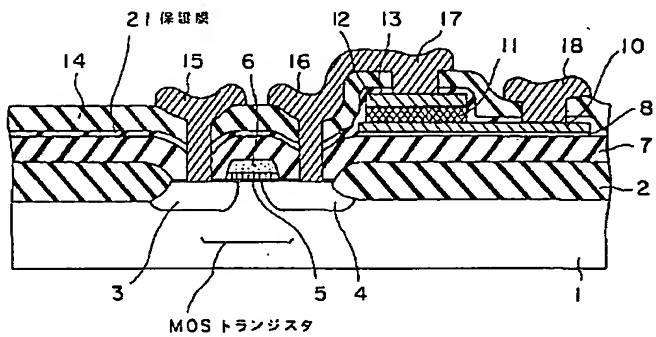
【符号の説明】

１…シリコン基板、　２…素子分離領域、　３…ソース領域、　４…ドレイン領域、　５…ゲート絶縁膜、　６…ゲート電極、　７…ＢＰＳＧ膜、　８…接着層、　９…強誘電体薄膜キャパシタ、　10…下部電極、　11…強誘電体薄膜、　12…上部電極、　13，21，41，51，61，82…保護膜、　15～18…取出し配線、　81…コンタクトホール。

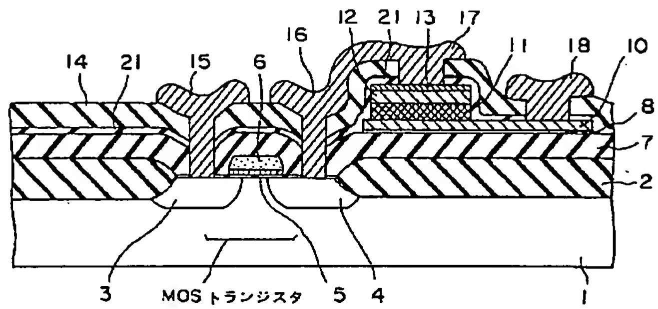
【図1】


上部電極 12
13 保護膜
取出し配線 16
取出し配線 17
取出し配線 15
ゲート電極 6
9
11 強誘電体薄膜
18 取出し配線
層間絶縁層 14
10 下部電極
8 接着層
7 BPSG膜
2 素子分離領域
2
3
MOS トランジスタ
5
4
1 Si 基板

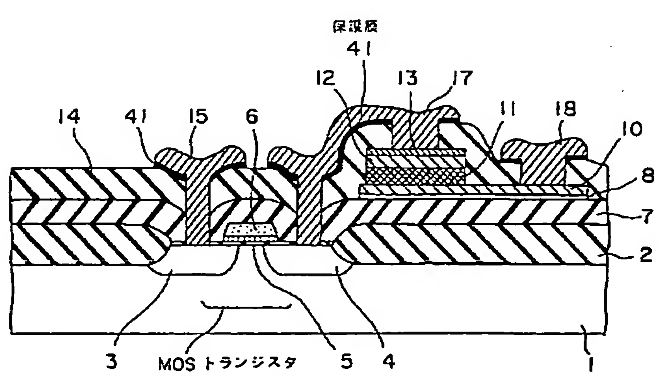
【図2】


21 保護膜
14
15
6
16
12
13
17
11
18
10
8
7
2
3
MOS トランジスタ
5
4
1

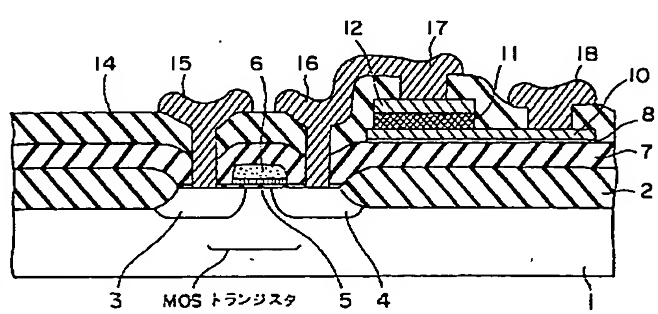
【図3】


14
21
15
6
16
12
21
13
17
11
18
10
8
7
2
3
MOS トランジスタ
5
4
1

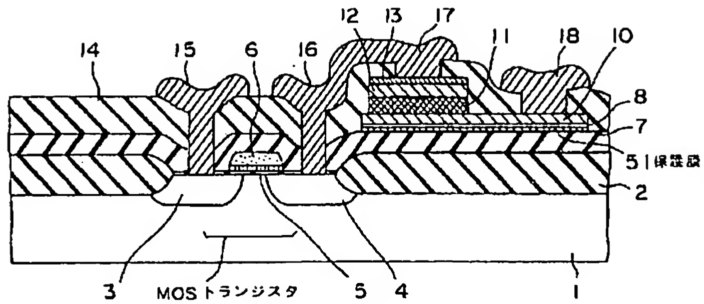
【図4】


保護膜
41
14
41
15
6
12
13
17
11
18
10
8
7
2
3
MOS トランジスタ
5
4
1

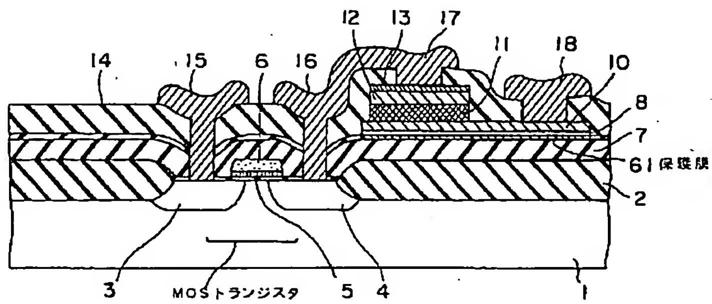
【図7】


14
15
6
16
12
17
11
18
10
8
7
2
3
MOS トランジスタ
5
4
1

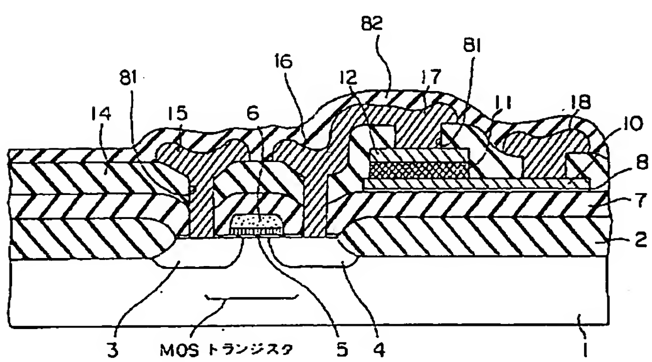
【図5】



【図6】



【図8】



フロントページの続き

(51) Int.Cl.^{6}	識別記号	庁内整理番号	F I	技術表示箇所
H01L　21/822				
21/8242				
27/108				

(72)発明者　渡辺　均
東京都渋谷区幡ヶ谷2丁目43番2号　オリンパス光学工業株式会社内

(72)発明者　黒田　吉己
東京都渋谷区幡ヶ谷2丁目43番2号　オリンパス光学工業株式会社内

(72)発明者　田所　かおる
東京都渋谷区幡ヶ谷２丁目43番２号　オリンパス光学工業株式会社内